The Design of a 2.7 V, 200 MS/s, and 14-bit CMOS D/A Converter with 63 dB of SFDR Characteristics for the 90 MHz Output Signal

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SUMMARY This paper describes the design of a 2.7 V operational, 200 MS/s, 14-bit CMOS D/A converter (DAC). The DAC consists of 63 current cells in matrix form for an upper 6-bit sub-DAC, and 8 current cells and R-2R ladder resistors for a lower 8-bit sub-DAC. A source degeneration resistor, for which a transistor in the triode operational region is used, is connected to the source of a MOS current source transistor in a current cell in order to reduce the influence of threshold voltage (Vth) variation and to satisfy the differential nonlinearity error specification as a 14-bit DAC. In conventional high-speed and high-resolution DACs that have the same design specifications described here, spurious-free dynamic range (SFDR) characteristics commonly deteriorate drastically as the frequency of the reconstructed waveform increases. The causes of this deterioration were carefully examined in the present study, finding that the deterioration is caused in part by the input-data-dependent time-constant change at the output terminal. Unexpected current flow in parasitic capacitors associated with current sources causes the change in the output current depending on the input data, resulting in time-constant change. In order to solve this problem, we propose a new output circuit to fix the voltage at the node where the outputs of the current sources are combined. SPICE circuit simulation demonstrates that 63 dB of SFDR characteristics for the 90 MHz reconstructed waveform at the output can be realized when the supply voltage is 2.7 V, the clock rate is 200 MS/s, and the power dissipation is estimated to be 300 mW.

key words: High-speed DAC, Low-voltage DAC, High-resolution DAC, CMOS DAC, SFDR characteristics

1. Introduction

High-speed and high-resolution DACs are used in graphics terminals and DDS (Direct Digital Synthesis) applications. In graphics terminal applications, high-end work station and ultra high resolution displays having more than $2000 \times 1500$ pixels are the target for the DAC. Here, the clock rate exceeds 200 MS/s, requiring a resolution of more than 12-bits. In DDS application, DACs with more than 12-bit resolution and more than 200 MS/s of operational capability are strongly required. However, low distortion of the reconstructed waveform up to Nyquist frequency is the most important characteristic [1]. DAcS with 14-bit resolution or 200 MS/s operation have been realized by using conventional CMOS technology [2]~[6]. MOS realization is desirable because these DACs will be installed in a system LSI. However, difficulties exist in realizing more than 14-bit and more than 200 MS/s operation while retaining superior spurious free dynamic range (SFDR) characteristics. In this paper, we try to resolve these difficulties.

Fourteen-bit resolution requires the good linearity at low frequencies. We call this specification "static linearity". Static linearity depends on device mismatch such as threshold voltage and transconductance parameter variation, and dimensional variation of the gate length and gate width of the transistors. These errors are both random and systematic. In order to equalize systematic error, a method such as the $Q^2$ random walk has been proposed [2]; however, it is very complicated and should be avoided if possible.

SFDR usually deteriorates rapidly with an increase in output signal frequency. One of the major causes of this nonlinearity has been thought to be a signal-dependent glitch that is generated due to the timing variation when current switches become on and off [3]. So far, the improvement in SFDR characteristics have not been sufficient. Therefore, another cause of SFDR degradation should be investigated for the sake of its further improvement.

Being pushed by the requirements, we have tried to design a 14-bit and 200 MS/s CMOS DAC with superior SFDR characteristics. Section 2 explains the block diagram of the conventional DAC. In section 3, a method to realize accuracy of 0.2 % for a current source is introduced. Section 4 shows the poor SFDR frequency characteristics of a conventional DAC. Section 5 again examines the conventional SFDR improvement techniques. Section 6 introduces the new cause of SFDR degradation and its improvement technique, which is developed in this study. Section 7 shows the improved SFDR frequency characteristics of the designed DAC. Section 8 concludes the study.
2. Block diagram of a 14-bit DAC

Figure 1 shows the block diagram of a conventional 14-bit CMOS DAC. It is constructed by combining the upper 6-bit sub-DAC which contains current-cells in matrix form with the lower 8-bit sub-DAC which contains R-2R ladder resistors [7]. The upper 6-bit sub-DAC consists of input decoders that convert the 6-bit input binary data into thermometer codes, 14 latches, 63 identical current sources each of which has accuracy of 0.2% or less, 63 selectors, and 63 identical current switches. Each current source becomes activated when the decimal number of the input data is increased by one. The lower 8-bit DAC consists of 8 input latches, 8 current sources each of which again has accuracy of 0.2% or less, 8 current switches, and R-2R ladder resistors. Binary weighting of currents are given by the R-2R ladder resistors. The output currents of the upper 6-bit sub-DAC and the lower 8-bit sub-DAC are combined at the output resistor \( R_{\text{out}} \) or \( R_{\text{out}}/w \), which is a part of the R-2R ladder resistors. It has differential outputs.

In this configuration, the accuracy required for the current source and the R-2R ladder resistors becomes 9-bit equivalent, that is, 0.2%, in order to obtain a differential nonlinearity error of less than \( \pm 1/2 \text{ LSB} \) in the 14-bit DAC. Therefore, it is realizable if a conventional CMOS process and current mirror circuits are used with appropriate care in realizing current sources.

3. A method for obtaining accuracy of 0.2 % or less in current sources

Each current source in the upper 6-bit sub-DAC and the lower 8-bit sub-DAC should have accuracy of 0.2% or less. We tried to obtain accuracy for the current source by adopting the source degeneration resistor scheme that places a resistor at the source terminal of a current source transistor. The influence of the \( V_{\text{th}} \) variation is reduced. Although the influence of the \( \beta \) variation becomes slightly high in the equivalent resistor part, it is still small compared with the \( V_{\text{th}} \) variation. Here, \( \beta \) is expressed as \( \mu C_{\text{ox}} W/L \), with \( \mu \), \( C_{\text{ox}} \), \( W \), and \( L \) being the mobility, the unit gate capacitor, the gate width, and the gate length of a transistor, respectively.

Figure 2 shows the concept of this. The input node voltage is fixed by an op amp so that it becomes equal to the output node voltage in a current mirror circuit. The conventional method of realizing a robust design for the \( V_{\text{th}} \) and \( \beta \) variation of a MOS current source is to use a long-channel transistor, that is, a transistor with a long gate length. The gate area thus increases and \( V_{\text{th}} \) and \( \beta \) variation are reduced. Because transconductance decreases the influence of \( V_{\text{th}} \), \( \beta \) variation decreases at the output. A long-channel MOS transistor is considered such that it consists of two different MOS transistors connected in series as shown in Figure 2. The lower parts of transistors M01, M11, and M22 are again considered as source degeneration resistors because they...
are operated in the triode operational region.

In this paper, the use of two separate MOS transistors in place of one long-channel MOS transistor is proposed as shown in Figure 3. The difference between the circuit seen in Figure 3 and that shown in Figure 2 is that the gate terminals of transistors M01, M11, and M22 in Figure 3 connect to another supply voltage $V_P$ which is higher than the voltage of gates of M0, M1, and M2. M01, M11, and M22 in Figure 3, of course, become the source degeneration resistors in the same manner as shown in Figure 2. Now, the influence of the parameter variation is assumed to be small, the amount of the gate-to-source voltage and the threshold voltage of M1 and M2, and M11 and M22, respectively.

We denote the $\beta$ and $V_{th}$ of transistors M1 and M2 as $\beta_1$, $V_{th1}$ and $\beta_2$, $V_{th2}$, respectively. We also denote the degeneration resistors of M11 and M22 as $R_1$ and $R_2$, respectively, and their average source voltage as $V_s$. As the parameter variation is assumed to be small, the source voltages of M1 and M2 become almost identical. Then, following the procedure described in reference 8, we obtain,

\[
\frac{\Delta I_d}{I_d} = \frac{-\Delta V_{thU}}{V_s + g_{mU}/2\beta_U} + \frac{g_{mU}/2\beta_U}{V_s + g_{mU}/2\beta_U} \left( \frac{\Delta \beta_U}{\beta_U} \right) - \frac{V_s}{V_s + g_{mU}/2\beta_U} \left( \frac{\Delta R}{R} \right) \tag{1}
\]

where, $\beta_U = (\beta_1 + \beta_2)/2$, $\Delta \beta_U = \beta_1 - \beta_2$, $R = (R_1 + R_2)/2$, $\Delta R = R_1 - R_2$, $I_d = (I_{d1} + I_{d2})/2$, $\Delta I_d = I_{d1} - I_{d2}$, $\Delta V_{thU} = V_{th1} - V_{th2}$, and $g_{mU}/\beta_U = V_{gsU} - V_{thU}$, $V_{gsU}$ and $V_{thU}$ are the average gate-to-source voltage and the threshold voltage of M1 and M2, respectively.

The degeneration resistor is formed by using a transistor in a triode operational region as shown in Figure 3. As $V_{th}$ and $\beta$ also varies in this transistor, the resistor value also varies. The relative error can be calculated as follows:

\[
\frac{\Delta R}{R} = \frac{\Delta V_{thR}}{V_P - V_{thR}} - \left( \frac{\Delta \beta_R}{\beta_R} \right) \tag{2}
\]

where $V_{thR}$ and $\beta_R$ are the $V_{th}$ and $\beta$ of a transistor used as a degeneration resistor.

The overall relative error is obtained by substituting equation (2) into (1). Now, let’s take the gate area of a transistor into account because the amount of the $V_{th}$ and $\beta$ variation is inversely proportional to the square root of the gate area. It then becomes convenient to express the relative error by converting it in the form of standard deviation. It becomes,

\[
\frac{\sigma (I_d)^2}{I_d^2} \simeq \frac{1}{V_s^2 L_W U_W} \times \left\{ \frac{\sigma (V_{thU})^2}{2} + \left( \frac{g_{mU}/2\beta_U}{V_s + g_{mU}/2\beta_U} \left( \frac{\Delta \beta_U}{\beta_U} \right) \right) \right. \\
\left. + \frac{1}{L_R W_R} \left( \frac{\sigma (V_{thR})^2}{(V_P - V_{thR})^2} + \left( \frac{\Delta \beta_R}{\beta_R} \right) \right) \right\} \tag{3}
\]

where $L_U$, $L_R$, $W_U$, and $W_R$ are the average gate length and the average gate width of transistors M1 and M2, and M11 and M22, respectively.

The first term in equation (3) indicates that the $V_{th}$ and $\beta$ variation of a transistor M1 or M2 are suppressed by the ratio of $1/V_s$ and $g_{mU}/2\beta_U V_s$. Usually, $V_s \gg (g_{mU}/2\beta_U)$ holds. The second term in equation (3) also indicates that the $V_{th}$ variation of a transistor used as a degeneration resistor is suppressed if $V_P \geq V_G$ compared with the circuit in the left side of Figure 2.

However, this comparison is not fair because the value of the degeneration resistor shown in Figure 3 is smaller than that in Figure 2 when $V_P \geq V_G$. In order to obtain the same degeneration resistor value, $W_R$ in Figure 3 should be set smaller than that in Figure 2 by the ratio of $(V_G - V_{thR})/(V_P - V_{thR})$. Substituting this ratio into the second term in equation (3) yields,

\[
2ndterm = \frac{1}{L_R W_R} \left\{ \frac{\sigma (V_{thR})^2}{(V_G - V_{thR})^2} + \frac{\sigma (\beta_R)^2}{(V_P - V_{thR})^2} \right\} \tag{4}
\]

Now, the degeneration resistor value of M11 or M22 seen in Figure 3 becomes equal to that of M11 or M12 in Figure 2. The effect is that the gate area of M11 or M22 in Figure 3 becomes smaller than that of M11 and M22 in Figure 2 by the ratio of $(V_G - V_{thR})/(V_P - V_{thR})$. $V_{th}$ variation is still suppressed as indicated by equation (4) because $V_P \geq V_G$. In this case, however, the $\beta$ variation increases by the ratio of $(V_P - V_{thR})/(V_G - V_{thR})$. The overall error, however, still decreases for the variation of the degeneration resistor value in Figure 3 compared with that in Figure 2 because the $V_{th}$ variation is dominant and is greater than the $\beta$ variation.

The accuracy of the current sources in different configurations are SPICE-simulated assuming the 0.35$\mu$m CMOS device parameters in order to verify the effectiveness of the proposed method and to confirm whether it can achieve accuracy of 0.2% or less. Table 1 shows the output current ($I_d$) variation with $V_{th}$, $W$, and $L$ as a parameters when $3\sigma$ values of variation is given to each parameter at random by using the Monte Carlo simulation method. W and L are a part of the $\beta$ and they represent the $\beta$ variation. Although there seems to appear two transistors M0 and M01, or M1 and M11 or M2 and M22 in Figure 2, it is actually one long-channel transistor. In order to obtain
TABLE I

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Fig. 2</th>
<th>Fig. 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{th}$ variation $(\pm 5mV)$</td>
<td>0.37 %</td>
<td>0.19 %</td>
</tr>
<tr>
<td>W/L variation $(\pm 0.035\mu m)$</td>
<td>0.054 %</td>
<td>0.081 %</td>
</tr>
<tr>
<td>Total</td>
<td>0.37 %</td>
<td>0.22 %</td>
</tr>
</tbody>
</table>

![Fig. 4](image_url) $I_{d1}$ variation of a circuit in Fig. 3

enough accuracy, 10 identical long-channel transistors are connected in parallel for realizing $M0$ and $M01$, or $M1$ and $M11$ or $M2$ and $M22$. The W/L ratio of one long-channel transistor out of 10 is $20\mu m/75\mu m$. The 3σ of $I_{d1}$ variation is tabulated in Table 1. The $V_G$ is chosen to be 1.2 V. Again, 10 identical transistors connected in parallel are used for $M0$ and $M01$, or $M1$ and $M11$ or $M2$ and $M22$ in Figure 3. The W/L ratios for one-tenth of $M0$ and one-tenth of $M01$, for example, are $12\mu m/4\mu m$ and $10\mu m/75\mu m$, respectively. $V_G$ is 1.2 V and $V_P$ is 1.9 V.

The data presented in Table 1 show that the total mismatch error is small for the circuit shown in Figure 3, although the total gate area is 53 % of that shown in Figure 2. The accuracy is almost the 9-bit equivalent, that is, 0.2 %, and this is sufficient to satisfy the differential nonlinearity error specification as a 14-bit DAC. However, error due to W and L variation tends to increase for transistors $M11$ and $M22$ in Figure 3. This is also consistent with the result of Equation 4. The error current histogram produced by the simulation is shown in Figure 4. As the $V_{th}$ variation is suppressed by using the degeneration resistor scheme and the influence of $\beta$ variation is thought to be small, we consider it to be unnecessary to introduce an equalizing procedure such as $Q^2$ random walk.

4. SFDR characteristics of a conventional DAC

The SFDR frequency characteristics of a conventional 14-bit CMOS DAC are shown in Figure 5. Figure 5 presents the circuit simulation results after designing each block shown in Figure 1. In this design, the latches of the upper 6-bit sub-DAC are connected directly to the input decoders and symmetrical switch control signals for a current switch are used. Therefore, no provision to reduce glitches has been adopted. We see similar frequency characteristics in the design shown in Van der Plas’s Figure 16 [2], although it does adopt some SFDR improvement techniques. In Figure 5, the frequency components of the output waveform as a result of a transient analysis are evaluated by applying the Fast Fourier Transform. The clock speed is 200 MHz and each current source has exactly the same current value as others in this simulation. The figure indicates that the SFDR degrades as the frequency of the reconstructed output waveform increases, and that the SFDR is only 53 dB for the 10 MHz output. This value is far smaller than the signal-to-noise ratio value of the ideal 14-bit DAC. Some means should be taken to improve such characteristics.

5. Conventional SFDR improvement techniques

The major cause of SFDR degradation is known to be glitch generation, which has two causes: variations in the timing of switch control signals at the current switch inputs, and changes in voltage at the common source terminal of switching transistors when the switch changes its state [5], [9].

Variations in the timing of switch control signals occur because of variations in the distance between the input latch and the current switch for each current source. Additional delay variations are introduced in a selector circuit depending on which input terminal the control signal is applied to. In order to alleviate this situation, the input latch is placed between the selector and the current switch as shown in Figure 6(a). As the latch’s output timing is synchronized with a clock, the on and off switch timing becomes equal for all of the
current switches.

The voltage change at the common source terminal of switch transistors is caused by applying the symmetrical control signals to switch transistors as shown in Figure 6(b). When \( V_{SW1} \) and \( V_{SW2} \) cross with each other at the halfway point of transition, the voltage \( V_s \) at the common source terminal changes. This causes additional current flow in the current source stray capacitors, and thus becomes a glitch at the output. To avoid this, the cross-point voltage of \( V_{SW1} \) and \( V_{SW2} \) is set high as shown in Figure 6(c). By using the setting in Figure 6(c), the change in \( V_s \) becomes small, thereby suppressing glitch generation.

As a result, the SFDR frequency characteristics are improved as shown in Figure 7 in which the bold line indicates 'with timing adjustment in current switching'. Although the improvement is about 10 dB in all the frequencies, this is still not a satisfactory value.

6. Extended SFDR improvement technique

In order to further improve the SFDR frequency characteristics, we tried to find other causes of SFDR degradation. By careful observation of the output waveforms, it becomes clear that time-constant change occurs at the output node of the DAC.

Figure 8(b) shows the rising time variation at the output of the DAC when the current flowing through the output terminal changes. The output waveform in Figure 8(a) is observed by converting this current into voltage by the output resistor. The input data are decremented one by one and the output voltage increases step by step. The rise time for a voltage change from 10% to 90% of each step is measured. When many current switches in the current cell matrix turn on, a large output current flows in the output; conversely, when only a small number of switches are on, a small current flows. Figure 8(b) indicates that the rise time depends on the output current and that the time increases with the increase of output current. The same kind of phenomenon is observed in measurements of the falling time.

The reason for the change in the rise time at the output is considered as follows and Figure 9 shows a possible solution.

In the current-cell matrix, each current source associated with a stray capacitor is connected to the load resistor \( R_{out} \) by way of a current switch. As the input data determine the on or off status of each of the current switches (from \( SW_1 \) to \( SW_{63} \)), the total number of stray capacitors connected to the load through a current switch also changes. In this case, however, a switch transistor doesn’t become the combination of an ideal switch and a resistor in series. Instead, it acts as a cascode transistor for a current source because the switch control voltage is limited to 2V max.
maximum. Although this configuration increases the output impedance of a current source, some current still flows through the stray capacitor when the voltage at $V_{out}$ changes by the step, because of the limited output impedance of a switch transistor. This additional current flow increases with the increase in the number of current switches turned on, and it decreases the output current $I_{out}$ flowing in the load resistor $R_{out}$. This causes the equivalent time-constant change at $V_{out}$ and the SFDR degradation at high frequencies, because the voltage step increases at high frequencies. To avoid this type of degradation, it becomes necessary to maintain the output voltage at a constant level.

The circuit that solves this problem is shown in Figure 10. The 64 current sources, including 1 dummy current cell, are grouped into 8 sections and each section thus ties 8 current source outputs through the current switches. In order to make these 8 current-cell output nodes constant, gain-boosted cascode circuits (from $M_1$ to $M_8$, and $Op_1$ to $Op_8$) are connected between the load resistor $R_{out}$ and the 8 current-cell output nodes. The voltages at the 8 current cell output nodes always equal $V_{ref}$, and they do not change with change in input data. The 8 drain terminals of the cascode transistors (from $M_1$ to $M_8$) are then connected to the load resistor $R_{out}$. Even when the voltage across the load resistor changes, all the outputs of the current cells are now isolated, and the stray capacitors in the current cells have no influence. The 8 drain terminals of the cascode transistors likewise have no influence because they are always connected to the load resistor.

Current sources are grouped into 8 sections as shown in Figure 10 in part because they are to be placed in $8 \times 8$ matrix form in the layout, and because the gate capacitance of a cascode transistor, for example, $M_1$, is small compared with that in the case when only one cascode transistor is used for all 63 current sources. When the gate capacitance of a cascode transistor increases, the time delay necessary for an op amp to control a cascode transistor in a gain-boosted circuit increases, and as a result, a large voltage spike is produced across the $R_{out}$. Although this spike does not depend on the input signal, since the time delay is constant, a large spike is not desirable. In order to avoid this situation, 8 gain-boosted cascode circuits are used rather than only 1. The use of 63 gain-boosted cascode circuits is desirable, however, as this greatly increases circuit and layout complexity, it is not a possible solution.

The gain-boosted cascode circuit is shown in Figure 11. $M_{n3}$ in Figure 11 corresponds to $M_1$, $\cdots$, or $M_8$ in Figure 10. $M_{n1}$, $M_{n2}$, $M_{p1}$ and $R_1$ form an op amp and $V_{b1}$ and $V_{b2}$ are the bias voltages. The source and gate terminals of $M_{n1}$ become the positive and inverted op amp terminals, respectively. $V_{ref}'$ is chosen 0.65 V and it is external. In this configuration, the voltage at terminal A, where the current source outputs are combined into one, becomes $V_{ref}' + V_{gs_{mn1}}$, and it is relatively constant, although it depends on the voltage gain of the op amp. In order to enhance the voltage gain and the frequency bandwidth of the
A current source that adopts a degeneration resistor scheme was developed. This possibly eliminates the use of the equalizing procedure for current sources. In addition to this, by eliminating the input-data-dependent time-constant change at the output terminal, the SFDR is improved by several dBs over the conventional SFDR improvement technique.

8. Conclusion

A 2.7V operational, 200MS/s, 14-bit CMOS DAC was designed by using 0.35um CMOS device parameters. A current source that adopts a degeneration resistor scheme was developed. This possibly eliminates the use of the equalizing procedure for current sources. In addition to this, by eliminating the input-data-dependent time-constant change at the output terminal, the SFDR is improved by several dBs over the conventional SFDR improvement technique.

References


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