A MONOLITHIC 10-BIT A/D & D/A CONVERTER FOR PCM AUDIO USE

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INTRODUCTION

In recent years, digital signal processing technique has become to be widely used in various electronics equipments. It allows the fidelity of the signal to be very high compared with that of conventional analog signal. For this purpose, A/D & D/A converters that digitize the analog signal accurately and reconstruct the digital codes into analog signal accurately are necessary.

Especially for A/D & D/A converters which deal with audio signal, those features as follows are required.
1) Needs relatively high resolution.
2) Coexistence of many analog circuits and digital circuits is necessary to perform dual channel conversion.
3) Conversion time is moderate such as 35KHz or 44KHz sampling.

A/D & D/A converters for PCM audio use which have been reported up to now 1),2) have very high resolution. However, one chip CODEC has not been reported yet. We report here a 10-bit monolithic A/D & D/A converter which is aimed at the application for recently announced 8mm Video etc.

We used dual slope integration scheme to perform both A/D & D/A conversion and gave the role of coarse integration to an upper 6-bit counter and fine integration to a lower 4-bit counter. Our bipolar process enables the IC to perform integration stable and to obtain high performance.

BLOCK DIAGRAM

Fig. 1 shows the block diagram of this newly developed IC. Dual-slope integration method is used both in A/D & D/A conversion. A coarse current source and a fine current source are prepared and both are used in common. Internal switches control those currents to be applied either to the A/D integrator or to the D/A integrator. The values of these current sources are fixed by an external resistor between VCC and IREF terminals. Each integrator consists of an analog switch for sample and hold purpose and a low-noise wideband operational amplifier. Different integrators are prepared one for A/D and another for D/A. An integration capacitor and resistors for discharge purpose of each integrator are external com-
ponents. Comparators No.1 and No.2 are also included in A/D part for the switching purpose of the fine current source (LSBs' current) and the coarse current source (MSBs' current), respectively.

In A/D mode, the incoming analog signal is applied to the external anti-alias filter (L.P.F.) by way of +6dB and buffer amplifiers. Left and right channel signals are then multiplexed by the switch to become the input of the A/D integrator.

In D/A mode, the output of the D/A integrator is time divided into left and right channel signals by the sample & hold amplifiers at the next stage. Each of these channel signals is buffered out and is applied to the external low-pass-filter, the same one as is used in A/D mode, for interpolation purpose.

Logic part consists of ECL logic such as shift registers, counters, and gates and controls the timing in A/D or D/A conversion. Data terminal is bidirectional, and outputs 10-bit data in A/D mode and inputs data in D/A mode. Switching control signal for left and right channel selection is applied to the Word terminal, while shift clock by which data is read or written to the Bit terminal. R/P terminal changes the mode form A/D to D/A or vice versa. Muting terminal has the function to force the data output to be all zeros both in A/D & D/A mode. Stand-by terminal has a role of reducing power by cutting off currents when the chip is neither in A/D mode nor in D/A mode.

OSC terminal is used to apply the master clock, for example, 11.6MHz to the chip. Only 1Vp-p is enough to get
the proper operation.

INTEGRATION PRINCIPLE

Fig. 2 shows the principle of A/D & D/A integration. We precede the explanation about A/D at first. When Word clock (Word terminal input signal) is high, the system should output the left channel data, therefore, integration for right channel input analog signal is performed as is shown in the figure. At the beginning of conversion, holding of the signal to which the integrator has tracked in previous cycle is done. In the interval, the left channel data which has been obtained by the conversion process in the previous cycle is transferred to output registers, and counters which count up integration period are initialized.

Subsequently, the coarse current source becomes to be on and counting starts. Once the output voltage level of the integrator exceeds the threshold $V_T$, comparator No.2 detects the level and forces the coarse current source off, instead, the fine current source becomes to be on. Until the output of the integrator reaches $V_{REF}$, integration by the fine current and counting continue. Just after reaching $V_{REF}$, comparator No.1 detects it and forces the current off completely, therefore, the output level of A/D integrator comes to be holded again. The output data $D_0$ is equal to INT ($C_A \times V_S$) / ($I_L \times t_{CK}$).

Where

- $C_A$: A/D integration capacitor value
- $V_S$: holded input signal level
- $I_L$: fine current source value
- $t_{CK}$: the time interval of the master clock

![Fig. 2 INTEGRATION SCHEME](image-url)
See Fig. 3 in detail.
After completing conversion, the integrator proceeds to track the another channel input signal and prepares for the next conversion.
For D/A integration, discharge to the voltage level which is set by external resistors of the D/A integrator is performed at first. Subsequently, coarse and fine currents become to be on at the same time and this integration continues during the period proportional to the input data value. The output level of the integrator \( V_{OUT} \) is given by

\[
V_{OUT} = \frac{I_L}{C_D} \cdot t_{CK} (2^nM + L)
\]

Where
- \( C_D \): D/A integration capacitor value
- \( M \): MSBs' data value in decimal
- \( L \): LSBs' data value in decimal
- \( I_L \), \( t_{CK} \): the same as those of A/D

At the end of the level is done automatically because current sources are switched off.
During this holding interval, sample and hold circuits at the next stage get the level out of the integrator output. After finishing this, the integrator begins to prepare for another channel conversion.

INTEGRATOR CIRCUIT

Each integrator consists of an analog switch and an operational amplifier. Moreover, the analog switch includes an amplifier and switching transistors (Q1 and Q2 in Fig. 4). In sample mode, amplifier \( A_1 \) together with Q1 and Q2 forms the closed loop. This means that Q1 and Q2 act as a simple buffer amplifier.
The analog signal (A/D mode) or the constant voltage applied to the IN terminal in Fig. 4(a) (D/A mode) is amplified by the next inverting input amplifier A2 with external resistors R1 and R2. The charge proportional to the input voltage is accumulated in the integrating capacitor at this time.

In hold mode (includes integration interval), the output of the amplifier \( A_1' \) equals to \( V_{REF} \) and the inverting input voltage level of the amplifier A2 also comes equal to \( V_{REF} \). As a result, Q1 and Q2 cut off (Fig. 4(b)). At the same time, as current sources are connected to the inverting input of the amplifier A2, charge which has been stored in the integration capacitor begins to decrease. Accordingly, the output voltage of A2 rises along with the straight line proportional to discharge current. Integration interval is controlled by comparators (A/D mode) or data values (D/A mode) by means of several switches.
Detailed circuit diagram of this analog switch and integrator is shown in Fig. 5.

CURRENT SOURCE CIRCUIT

Fig. 6 shows the current source circuit that produces the coarse current and the fine current. The current ratio of these is selected to be 16:1. This is because we decided to give the role of coarse integration to a 6-bit counter and fine integration to a 4-bit counter. The circuit consists of an operational amplifier and current mirrors.
As the voltage at non-inverting input terminal \( I_{REF} \) of the op-amp comes equal to \( V_{REF} \), the current \( I_R \) which flows through the transistor Q3 is decided to be

\[
I_R = (V_{CC} - V_{REF})/R_{EX}
\]

Where \( R_{EX} \) is an external resistor. When the base voltage of Q3 is applied to current mirror transistors Q4 and Q5, we can get

\[
I_{MSB} = \frac{I_R}{16} = I_{LSB}
\]

COUNTER CIRCUIT

Counters and shift registers that perform counting of input data and stores data from counters are connected in such a way as is shown in Fig. 7. The main purpose here is to reduce...
$I_M = 16 I_L$
$C_D = (16M + L)$
$= \text{int}[\frac{C_A}{I_L} \cdot t_{CK}]$

**Fig. 3 A/D INTEGRATION**

**Fig. 4 S/H CIRCUIT**

**Fig. 5 ANALOG SWITCH AND INTEGRATOR**
elements count, and the flow of data comes to be bi-directional in order to perform the function with minimum components. When in A/D mode, LR signal precedes LD signal. Thus, transfer of data from TFF counter to SREG shift register is done at first. The LD initializes TFF counter preparing for counting in integration interval.

P (preset) input of TFF is always at zero level in A/D mode, therefore, Q out becomes to be zero when LD becomes high.

On the other hand, in D/A mode LR stays low. No data at P (preset) input of SREG is able to enter into the shift register in this case. Instead, data at Q out is transferred to the TFF when LD becomes high.

In this way, the same counters and registers are used both for A/D & D/A conversion in common.

IC PERFORMANCE

Fig. 8 and Fig. 9 show the frequency characteristics of this newly developed IC. Output level, total harmonic distortion, and L/R separation curves of D/A converter are plotted in Fig. 8. T.H.D. curve shows that the D/A has full 10-bit resolution, while separation is good enough not to affect the accuracy. Aperture effect is seen in the curve of the output level. Compensation shall be done by the external filter. The degradation of harmonic distortion in frequency range above 10KHz is mainly due to the aliasing. External filter don't have enough attenuation over the range of 15KHz.

In measurement of the D/A converter, sinusoidal wave data is inputted to the IC from a memory.

T.H.D. and separation curves of A/D and D/A back-to-back response are plotted in Fig. 9. In this case, data curve can't reveal the characteristics better than that of D/A only. The data can well be accepted for 10-bit A/D & D/A conversion. Overall characteristics are summarized in Table-1. 10-bit resolution has been obtained at the conversion rate of 31.5KHz. S/N and
T.H.D. values are very close to the theoretical one. Power dissipation in stand-by mode reduces to 60mW while it is 160mW in conversion mode. Total elements count reaches to about 2,700. The chip is fabricated in Toshiba's A-NSA bipolar process and is installed in a 44 pin flat package. Fig. 10 shows the die photograph of this newly developed IC.

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REFERENCES


| Resolution | 10 bits |
| Conversion Rate | 31.5 kHz |
| Master Clock Frequency | 11.6 MHz |
| Number of Channels | 2 |
| S/N | 60 dB |
| T.H.D. | 0.1% |
| Supply Voltage | 5 V |
| Element Counts | 2,700 |
| Power Dissipation | Conversion Mode 160 mW |
| Channel Separation | Stand-by Mode 60 mW |
| Chip Size | 4.7 x 4.0 mm² |
| Fabrication Technology | Bipolar |
| Package | Flat Package 44 pin |

Table-1. IC PERFORMANCE

Fig.8 D/A FREQUENCY CHARACTERISTICS

Fig.9 BACK TO BACK FREQUENCY CHARACTERISTICS
**Fig. 10** DIE PHOTOGRAPH

**BIOGRAPHIES**

Mr. Yasuhiro Sugimoto received the B.S.E.E. in electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan in 1973, and the M.S.E. in computer aided design from the University of Michigan, Ann Arbor, Michigan in 1980. In 1973 he joined Toshiba Corporation where he has been involved in the development of new technologies for analog integrated circuits. During 1979-1980 he was on leave at the University of Michigan, Ann Arbor, Michigan, where he worked on the computer aided circuit design for integrated circuits. Mr. Sugimoto is a member of the Institute of Electronics and Communication Engineers of Japan.
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