A 1 MHz, Synchronous, Step-down from 3.6 V to 1 V, PWM CMOS DC-DC Converter with more than 80% of Power Efficiency

Yasuhiro SUGIMOTO†, Member and Shinichi KOJIMA††, Nonmember

SUMMARY This paper introduces a power-efficient on-chip DC-DC converter, which produces a 1.0 V output by being stepped-down from a 3.6 V input, utilizes a 10 µH external inductor, and realizes more than 80% power-efficiency. In order to realize a 1.0 V output without decreasing power-efficiency, a synchronous-type rectifier scheme with a reverse current protection circuit is adopted and a reference voltage of less than 1.0 V is developed. The external inductor value is reduced by applying the PWM control scheme and a new low-power 1 MHz triangular waveform oscillator. High-value resistors are used in analog circuits including a voltage reference, a triangular waveform oscillator, an error amplifier, and a comparator to have the ultra-low power characteristics. A chip is actually designed and fabricated by using the 2 µm CMOS process. As a result, a 1 MHz, synchronous, step-down from 3.6 V to 1 V, PWM DC-DC converter has been realized with a power efficiency of more than 80% in the output current range from 40 to 70 mA.

key words: step-down DC-DC converter, 1 MHz operation, 1 V output, power efficiency, PWM

1. Introduction

Step-down DC-DC converters have seen increasing popularity in their utilization in various kinds of mobile equipments. In the case of a mobile phone, for example, the LSIs’ power supply, whose voltage is approximately 1.5 V, is supplied by a lithium-ion secondary battery. As the voltage of a lithium-ion secondary battery is more than 3 V, it is necessary to step down the voltage to the one of LSIs.

Series regulators have been frequently used to step down the voltage [1]–[3] because such regulators don’t generate the noise associated with switching. However, they aren’t suitable for use when the input and the output voltage ratio is large. A large amount of power is dissipated in the output transistor because the voltage difference between the input and the output becomes the drain-to-source voltage of the transistor.

In contrast to this, a switching-type converter such as a DC-DC converter is widely used when the input and the output voltage ratio is large [4]. In a DC-DC converter, the output transistor acts as a switch and its drain-to-source voltage difference becomes small when the switch turns on. Therefore, the power dissipation is small. The power efficiency of a DC-DC converter is high compared with that of a series regulator. Although a large switching noise is generated, the DC-DC converter is frequently used in a mobile phone because of the importance of the battery’s lifetime. The power efficiency of a conventional DC-DC converter, however, is limited by the power loss of the external diode, which is connected between the ground and the drain of the output transistor.

In order to realize a 1.0 V output, a voltage of 1.0 V as a reference, and a triangular waveform oscillator whose oscillation frequency is stabilized by using the reference voltage, are needed. An oscillation frequency of more than 1 MHz is desirable. When the oscillation frequency increases, the energy stored in an external inductor per cycle becomes small. Therefore, an external inductor with a low inductance value can be used, allowing its size to be small [5].

Aiming the realization of a DC-DC converter IC which is suitable for use in mobile equipments, a power-efficient on-chip DC-DC converter with more than 80% power-efficiency, with a 1.0 V output stepped-down from a 3.6 V input, and with 10 µH of external inductor has been designed and fabricated by using 2 µm CMOS technology. This paper evaluates the performance of this design, thus demonstrating its effectiveness and usefulness of this IC. In Sect. 2, a DC-DC converter that adopts a PWM approach is introduced. Section 3 develops circuits that enable the 1.0 V output without decreasing the power efficiency. Section 4 describes a stable 1 MHz oscillation and an oscillator circuit. Section 5 shows the experimental results and provides a discussion of what part of the DC-DC converter IC is critical in obtaining an increase in power efficiency. Finally, Sect. 6 concludes the paper.

2. A DC-DC Converter that Adopts the PWM Approach

The converter adopts the PWM approach as shown in Fig. 1 [6]. The most important feature of the PWM approach is that it has a fixed interval for the control signal to allow the output voltage to be kept constant. The harmonics contained in the waveform of Vout as ripple components become discrete and fixed in frequency; therefore, their influence on other functional blocks can be minimized. The negative feedback loop is formed by using an error amplifier, a PWM-type comparator, a control circuit, output transisors Mp and Mn, an external inductor LEX, an external capacitor CEX, and a load resistor Rload as shown in Fig. 1.
When the output voltage is lower than the reference voltage \( V_{\text{ref}} \), whose value is chosen to 1.0 V and is independent of supply voltage and temperature changes, the output of the error amplifier becomes positive. A PWM-type comparator then compares the output voltage of the error amplifier with the voltage of a triangular waveform oscillator in Fig. 1. The more the output of the error amplifier becomes positive, the more the output pulse width of the PWM-comparator increases. This lengthens the time interval when \( M_p \) becomes on and, as a result, the \( V_{\text{out}} \) increases. When \( V_{\text{out}} \) approaches \( V_{\text{ref}} \), the pulse width at the output of a PWM-type comparator decreases and the pulse finally diminishes when \( V_{\text{out}} \) exceeds \( V_{\text{ref}} \). The oscillation frequency of the triangular waveform oscillator is determined by the hysteresis voltage which is produced by using the reference voltage \( V_{\text{ref}} \). Therefore, it is also independent of supply voltage and temperature changes. The NMOS transistor \( M_n \) instead of a conventional external shottkey diode is used in the output stage.

3. Circuits that Realize a 1.0 V Output

In order to realize the 1.0 V output voltage, a synchronous-type rectifier shown in Fig. 2 is used. When the energy is stored in an external inductor \( L_{\text{EX}} \), \( M_p \) turns on and the charging current \( I_{\text{ch}} \) flows in the direction shown in Fig. 2. When \( M_n \) turns on, an external inductor begins to release its energy. In this time interval, the current flows in a loop of the inductor \( L_{\text{EX}} \), the load resistor \( R_{\text{load}} \), and the \( M_n \) in the direction ‘Forward’ as indicated in Fig. 2. In both cases, the on-resistance of a MOS transistor is small, for example 1\( \Omega \), and the voltage across a MOS transistor becomes small. Therefore, the power consumption in MOS transistors is low.

However, the configuration shown in Fig. 2 has two drawbacks. The first is that the through current flows from \( V_{\text{in}} \) to ground by way of \( M_p \) and \( M_n \) on the transition when \( M_p \) turns on and \( M_n \) turns off or vice versa, and thus increases power consumption. In order to eliminate the through current, a pulse control circuit as shown in Fig. 2 is designed. The circuit produces a non-overlapping control signal as shown in Fig. 3 for \( M_p \) and \( M_n \) by using delay elements between logic gates.

Another drawback is the generation of the reverse current flow, which occurs under a light load condition. When the load is light, the energy stored in an inductor is small. This energy is released to the load when an NMOS transistor \( M_n \) turns on. However, the energy is discharged in a short time and the discharge current \( I_{\text{dis}} \) flows in the direction labeled ‘Reverse’ as shown in Fig. 2 during the rest of the clock interval. The reverse current uses the energy stored in \( C_{\text{EX}} \), and it should be avoided by turning off the \( M_n \). The phenomena can be detected by monitoring the voltage at terminal \( IC_{\text{out}} \) in Fig. 2. When \( I_{\text{dis}} \) current flows in the direction labeled ‘Forward,’ the voltage at terminal \( IC_{\text{out}} \) becomes negative because the source terminal of \( M_n \) is connected to the ground and the current flows from the source terminal to drain terminal. On the other hand, when the reverse current flows, the voltage at terminal \( IC_{\text{out}} \) changes from minus to plus because the current flows from the drain terminal to the source terminal at this time.

In order to detect the reverse current flow and turn off the \( M_n \) when it is detected, a comparator, which compares the voltage at terminal \( IC_{\text{out}} \) and the ground level, and a flip-flop are introduced. As shown in Fig. 3, a signal \( S \) for the negative-edged flip-flop is produced by the rising edge of the signal at terminal B in Fig. 2. The falling edge of the S signal sets the \( M_n \) on. Once the reverse current is detected, the comparator is activated and the R signal goes low. This forces \( M_n \) to turn off as shown in Fig. 3, and the reverse current flow ceases. The R signal is forced to be high by using the signal at terminal B when \( M_n \) turns on in order to avoid the influence of the comparator output change during this time.

The reference voltage circuit should supply the stable 1.0 V of voltage to the error amplifier and the constant currents to the oscillator as shown in Fig. 1. Figure 4 shows the circuit of the reference voltage circuit. It produces the stable 1.0 V as \( V_{\text{ref}} \), which is independent of \( V_{\text{in}} \) and temperature changes. We already know that the bandgap reference voltage circuit can produce voltage which is independent of supply voltage and temperature changes. However, its voltage is approximately 1.2 V. Dividing the 1.2 V into 1.0 V by using resistors increases the power consumption; therefore, this isn’t preferable.

In Fig. 4, \( V_{\text{ref}} \) is determined by,

\[
V_{\text{ref}} = \left( 1 + \frac{R_2}{R_1} \right) V_{\text{gs}M_2} \tag{1}
\]

\[
V_{\text{gs}M_2} = V_{\text{th}2} - \left( \frac{\sqrt{\beta_1}}{\sqrt{\beta_2}} \right) V_{\text{thd}} \tag{2}
\]

Where \( \beta_1 = \beta_2 \), \( \beta_1 \) and \( \beta_2 \) are transconductance parameters of transistors \( M_1 \) and \( M_2 \), and \( V_{\text{thd}} \) is the threshold voltage of \( M_2 \). We used the depletion-type transistor for \( M_1 \) as shown in Fig. 4; therefore, the threshold voltage \( V_{\text{thd}} \) becomes negative. The temperature dependence of \( V_{\text{thd}} \) is such that it increases the value in the negative direction when the temperature rises. \( M_2 \) is a low-Vth and enhancement-type
transistor and $V_{gsM2}$ can be set to less than 1 V although the second term of Eq. (2) becomes positive. Equation (2) indicates that $V_{gsM2}$ is insensitive to the temperature change because the temperature dependence of $V_{th}$ of a depletion-type transistor $M_1$ is the same as that of an enhancement-type transistor $M_2$ [7], [8]. As $I_1$ and $I_2$ are constant current sources, $V_{gsM2}$ becomes independent of both the temperature and the supply voltage changes. The resistor values of $R_1$ and $R_2$ were set as high as 1 MΩ in order to reduce the power.

4. A Low-Power Oscillator Circuit and 1 MHz Operation

The operation frequency of the previous generation DC-DC converters was around several hundreds of KHz. In that case, the external inductor value becomes about 20 to 50 µH. If the DC-DC converter can operate at 1 MHz, the inductor value could be as low as 10 µH [9], thus reducing the cost and the space of the converter module. In order to achieve 1 MHz operation, circuit currents must be increased. As this leads to a decrease in power efficiency, a 1 MHz oscillator that consumes power equivalent to or less than its previous counterpart is needed. That is, a stable triangular waveform oscillator whose frequency and amplitude are independent of temperature and supply voltage changes is needed. Figure 5 shows the circuit of a triangular waveform, relaxation-type oscillator [10]. The voltage waveform across a capacitor $C_T$ becomes triangular in shape. The $C_T$ is charged and discharged by the constant current sources $I_1$ and $I_2$ that are generated by using the constant voltage of the reference voltage generator and are independent of the supply voltage and the temperature changes. When the voltage across the $C_T$ reaches the upper threshold voltage, the switch $S_5$ turns on and the $C_T$ is discharged. When the voltage across the $C_T$ reaches the lower threshold voltage, the switch $S_4$ turns on and the capacitor is charged.

These threshold voltages should be stable in order to obtain a fixed oscillation frequency. Threshold voltages are produced by utilizing stable reference voltages. However, a conventional relaxation-type oscillator uses resistors and analog switches to produce the upper and the lower threshold voltages and, therefore, consumes power. In Fig. 5, threshold voltages are produced by using capacitors and switches. When switches $S_1$ and $S_3$ are on, the stable reference voltage $V_{ref}$ is applied to the capacitor $C_{r1}$ and this voltage becomes the upper threshold voltage. When the capacitor voltage of $C_T$ exceeds the upper threshold voltage, switches $S_1$ and $S_3$ turn off and $S_2$ turns on. The charge stored in $C_{r1}$ is distributed to both $C_{r1}$ and $C_{r2}$. This voltage becomes the lower threshold voltage and is half of the $V_{ref}$ when $C_{r1}$ equals $C_{r2}$. Because the voltage across the capacitor $C_T$ goes up and down between the upper and lower
threshold voltages, and because current sources $I_1$ and $I_2$ supply the constant currents at any time, stable oscillation is realized. In this configuration, dc current doesn’t flow to produce the upper and lower threshold voltages. Thus, a low-power operation is achieved while the circuit operates at 1 MHz.

The error amplifier produces a pulse-like waveform when the voltage at $V_{out}$ in Fig. 1 becomes low relative to the reference voltage $V_{ref}$. It is the ac amplifier. The error amplifier requires a phase margin and the voltage gain at 1 MHz. The phase margin is necessary in order to avoid oscillation because the feedback loop is formed to stabilize the output voltage. As shown in Fig. 1, an operational amplifier with $1.0 \text{ V}$ of $V_{ref}$ which is connected to the positive input terminal, with the voltage $V_{out}$ which is connected to the negative input terminal by way of an external resistor, and with an external feedback capacitor and a resistor in series between the output terminal and the negative input terminal is used as an error amplifier. The frequency characteristic is determined by these external resistors and a capacitor, which is in a lag-lead configuration. According to the simulation that utilizes device parameters of $2 \mu\text{m}$ CMOS technology, the voltage gain at 1 MHz is 29.5 dB, and the phase margin at the frequency where the voltage gain becomes zero is 48.1 degrees as shown in Fig. 6.

5. Experimental Results

A 1 MHz, synchronous, step-down from 3.6 V to 1 V, PWM CMOS DC-DC converter was designed and fabricated by using $2 \mu\text{m}$ CMOS technology. This process offers a depletion-type MOS transistor, a low-Vth MOS transistor, and a high-value resistor [11].

Figure 7 shows the measured power dissipation in each block of this DC-DC converter IC. The power consumption of analog circuit blocks such as an error amplifier, a reference voltage generator, an oscillator, and a comparator is minimized. It was only 1.01 mW when $V_{in}$, $P_{in}$, $V_{out}$, and $P_{out}$ are 3.6 V, 95.7 mW, 0.97 V, and 77.5 mW, respectively. Most of the power dissipation is in the output part, which includes the output transistors and their buffers. The on-resistance of the PMOS and NMOS transistors, and the series resistance of an external inductor were measured as 1.32 $\Omega$, 0.48 $\Omega$, and 0.37 $\Omega$, respectively. When the time interval in which PMOS and NMOS transistors are on is 0.3 $\mu\text{s}$ and 0.6 $\mu\text{s}$ out of one clock period of 1 $\mu\text{s}$, respectively, the average currents that flow through the PMOS transistor, NMOS transistor, and an external inductor becomes 26.5 mA, 54.3 mA, and 80 mA, respectively. Therefore, the power dissipation in the PMOS transistor, NMOS transistor, and an external inductor are calculated as 3.1 mW, 2.4 mW, and 2.4 mW, respectively. The sum of these is, however, only 7.9 mW, which is half of the measured power consumption in the output stage. There must thus be another cause of power dissipation.

Stray capacitors associated with output power transistors are considered to be possible cause. Figure 8 shows stray capacitors and their states when they have been charged or discharged when PMOS is turned on and NMOS is turned off (Fig. 8(a)), and when NMOS is turned on and PMOS is turned off (Fig. 8(b)). In Fig. 8(a), for example,
charged by way of PMOS. As the reverse voltage is applied, half of the energy which is supplied from the power supply is consumed in a resistor and the remaining half is stored in a capacitor. When a capacitor is discharged through a resistor afterward, the stored energy in a capacitor is dissipated in the resistor. Therefore, in Fig. 8, in total, the energy dissipated by \( C_{dbp} \) per cycle is calculated as \( C_{dbp} V_{in}^2 f \). Likewise, \( C_{dbp}, C_{dn}, \) and \( C_{gsn} \) dissipate \( C_{dbp} V_{in}^2, C_{dn} V_{in}^2, \) and \( C_{gsn} V_{in}^2 \), respectively, per cycle. However, \( C_{dp}, \) and \( C_{gdn} \) dissipate twice the power than usual because the charge stored in them changes polarity from the charge process to the discharge process and vice versa. For example, \( C_{dp} \) is charged in the polarity as shown in Fig. 8(a) when PMOS is turned on and NMOS is turned off. However, when NMOS is turned on and PMOS is turned off, \( C_{dp} \) is charged in reverse as shown in Fig. 8(b). Charge and discharge processes occur twice per cycle for \( C_{dp} \) and \( C_{gdn} \). From the discussion above, the total power dissipation by stray capacitors is calculated as,

\[
P_{dis} = V_{in}^2 f \\
\quad \times \left( C_{dp} + C_{dn} + C_{gsn} + 2 C_{gdp} + 2 C_{gdn} \right) \quad (3)
\]

where \( V_{in} \) and \( f \) are the input voltage and the clock frequency of a DC-DC converter and they are 3.6 V and 1 MHz, respectively, in this design. Among these capacitors, \( C_{dp}, C_{dn}, \) and \( C_{gdn} \) are junction capacitors while \( C_{gsn}, C_{dp}, C_{gs}, \) and \( C_{gdn} \) are gate-to-source and gate-to-drain capacitors of PMOS and NMOS transistors. The capacitance of a junction capacitor changes depending on the reverse bias voltage, and gate-to-source and gate-to-drain capacitors vary depending on the operating region of a MOS transistor. We assume that the threshold voltage \( V_{th} \) is small compared with \( V_{in} \) and that transistors stay in the triode operational region for most of the time they are on. Then, \( C_{gsn}, C_{dp}, C_{gsn}, \) and \( C_{gdn} \) are capacitors when PMOS and NMOS transistors are in the triode region and are estimated as 77 pF, 77 pF, 30 pF, and 30 pF, respectively. As the reverse voltage of the \( C_{dp} \) becomes zero in the case when PMOS is on, and becomes \( V_{in} \) in the case when NMOS is on, we take the stored charge of \( C_{dp} \) as that when the reverse voltage is \( V_{in} \). It is 16 pF. The situation is the same for \( C_{gdn} \), 6 pF.

By substituting these values into equation (3), we obtain 4.5 mW of power dissipation for transistors’ stray capacitors in the charging and discharging processes. The output part of the DC-DC converter is expected to consume 12.4 mW in total by calculation; it was actually 13.7 mW. It is evident that almost all the power dissipation is concentrated in the output part, including the buffers.

Figure 9 and Fig. 10 show waveforms at the terminal \( I_{out} \) in heavy load mode (\( I_{load} \) = 100 mA, horizontal: 200 ns/div, vertical: 2 V/div).

![Fig. 8](image1.png)

**Fig. 8** Power dissipation in stray capacitors (a) PMOS: on, NMOS: off, (b) PMOS: off, NMOS: on.

![Fig. 9](image2.png)

**Fig. 9** The voltage waveform at terminal \( I_{out} \) in light load mode (\( I_{load} \) = 10 mA, horizontal: 200 ns/div, vertical: 2 V/div).

![Fig. 10](image3.png)

**Fig. 10** The voltage waveform at terminal \( I_{out} \) in heavy load mode (\( I_{load} \) = 100 mA, horizontal: 200 ns/div, vertical: 2 V/div).
current doesn’t flow when the load current is 100 mA. This is the heavy load condition. Figure 10 verifies its proper operation. In this case, a PMOS turns on and an NMOS turns on next, during one clock period. The ripple across the capacitor $C_{EX}$ in Fig. 1, which is the rectified output of the waveform shown in Fig. 10, becomes less than 20 mVp-p.

Figures 11 and 12 show voltage waveforms in transient response across the capacitor $C_{EX}$ when the load current is increased or decreased by the step from a light load mode to a heavy load mode, or vice versa. Figure 11 shows that the response time when the load current changes from 10 mA to 100 mA by the step is about 10 µs, and Fig. 12 shows that the response time when the load current changes from 100 mA to 10 mA by the step is about 25 µs. In the case when the load changes from a light mode to a heavy mode, the voltage across the capacitor drops and the feedback loop is activated. Due to this feedback operation, the response time is shortened. On the other hand, in the case when the load changes from a heavy mode to a light mode, the voltage across the capacitor rises to more than 1 V. In this case, the comparator output is always low and no control signal is generated. Therefore, the output voltage across $C_{EX}$ is discharged gradually in a natural fashion by the current flowing in a load. The response time increases. The voltage continues to drop below 1 V and the feedback operation is activated again.

Figure 13 shows the frequency spectrum of the $V_{out}$ seen in Fig. 1. The level of the 1 MHz fundamental signal is 2.5 mVrms while the second harmonic is 0.7 mVrms and more than third harmonics are less than 0.2 mVrms. This indicates that the ripple of $V_{out}$ is small.

Figure 14 summarizes the overall power efficiency characteristics. The horizontal line is the load current and the vertical line shows the power efficiency. The upper bold line is the one when the 2.5 V input voltage is stepped down to 1.0 V, while the lower bold line is the one when the 3.6 V input voltage is stepped down to 1.0 V. The former is highly efficient because the current flowing in the external inductor has been reduced. The dashed lines indicate that the DC-DC converter is operating in a light load mode and achieving high efficiency by protecting the reverse current flow. With 3.6 V input and 1.0 V output voltages in the output current range from 40 mA to 70 mA, more than 80% power efficiency has been achieved. Even at an output current of 200 mA, the power efficiency remains at 75%.
6. Conclusion

A step-down DC-DC converter from 3.6 V to 1.0 V with 1 MHz operational capability and with more than 80% power efficiency has been realized by using 2 µm CMOS technology. Careful observation of the power consumption has been carried out in which part the power is consumed. The stray capacitors of the output transistors, logic circuits including buffers, on-resistances of the output transistors, and the series resistance of an inductor dissipate 4.7%, 4.0%, 5.8%, and 2.5% of the input power, respectively. In order to further increase circuit’s power efficiency, it is necessary to decrease the power consumption of the output part including the drivers and the transistor’s stray capacitors. This will be the focus of our future investigations.

References


Yasuhiro Sugimoto received the B.E. degree from Tokyo Institute of Technology, Tokyo, Japan, M.E. degree from University of Michigan, Ann Arbor, Michigan, and Doctor of Engineering degree from Tokyo Institute of Technology, Tokyo, Japan, in 1973, 1980, and 1991, respectively. He joined Toshiba Semiconductor Group in 1973, and has engaged in the development of analog VLSIs. Since 1992 he has been with the Faculty of Science and Engineering, Chuo University where he is now a professor in the Department of Electrical, Electronic, and Communication Engineering. His main interest is the design and development of new circuits in mixed-signal and RF LSIs. He is the recipient of the 1989 Best Papers Award of the European Solid-State Circuits Conference and the 1998 IEICE Best Papers Award. He is the author of three books. Dr. Sugimoto is a member of the Institute of Electrical and Electronics Engineers, INC., the Institute of Electrical Engineers of Japan, and the Japan Consulting Engineers Association.

Shinichi Kojima received the B.E. degree and M.E. degree both from Osaka University, Osaka, Japan, in 1986 and 1988, respectively. He joined Ricoh Electronic Devices Division in 1988, and has engaged in the development of Memory IC’s until 1995. Since 1996 he engaged in the development of Power Management IC’s especially of Switching Regulators, and now is a manager of No. 23 Design Section, Power Management 2nd Business Unit.