A 10-BIT 65MSPS GLITCH-FREE VIDEO D/A CONVERTER

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1. INTRODUCTION

In these days digital signal processing of video signal has become popular due to the development of monolithic video D/A and A/D converter. It is said that 8 bits resolution is sufficient for real time video signal processing such as digital T.V. application, however, 9 to 10 bits resolution is required to the use of digital VTR, camera and studio equipments.

The newly developed D/A converter LSI has 10 bits resolution and operates up to 65MHz sampling clock frequency and can be applicable not only for the application stated above but also for currently developing High Definition T.V..

2. BLOCK DIAGRAM OF D/A CONVERTER LSI

Figure 1 shows the block diagram of this newly developed LSI. It consists of 8 circuits as follows.

(1) R-2R Ladder Resistors +6 Constant Current Sources (Lower 6 bits), 15 Constant Current Sources (Upper 4 bits) and 21 Switchs.

(2) Input Buffer Circuits (ECL/TTL compatible).

(3) Binary to Hexa-decimal Decoder (Upper 4 bits).

(4) Latch Circuits

(5) Clock Driver Circuit.

(6) Bias Voltage Generation Circuit.

(7) Circuit for turning Inputs to be applicable to ECL or TTL.

(8) High Speed Amplifier for Aperture Correction.

Upper 4 bits of this LSI are segmented into 15 equally valued constant current sources, and the lower 6 bits, into R-2R ladder resistors and 6 constant-current sources.

The merits of this structure are mentioned as follows,

(1) The glitch inherent in D/A converter has been reduced to 1/16 of the conventional DACs.

(2) The accuracy required for devices, transistor's $\Delta V_{be}$ or deviation of the ratio of resistor value has been lowered to about 1/4 compared with the conventional DACs.

However, this type of DACs always requires a decoder circuit which converts
binary code to hexa-decimal code. High speed decoding with simple circuitry is required to this decoder. We have developed a new decoder circuit for this purpose as shown in Fig. 2.

3. HIGH SPEED DECODER CIRCUIT

S1, S2, S3 and S4 are switches which correspond to MSB, 2nd bit, 3rd bit and 4th bit of digital inputs, respectively. Making correspondence of switches in the left position to the "1" state of corresponding inputs and switches in the right position to the "0" state, the voltage level VA at point VA and VB at point VB can be shown as in Fig. 3 with upper 4-bits binary code in the horizontal line. Voltage levels V1 to V7 in Fig. 2 are also shown in Fig. 3 to help understanding.

Making use of Fig. 2 and Fig. 3, I explain the operation of this decoder circuit.

When input upper 4 bit binary code is 0000, all 15 current sources are in "OFF" state because the voltage level VA exceeds those of V1 to V7.

Once input binary code changes to 0001, V1 becomes higher than VA and, consequently, only one current source becomes to be "ON" state.

In this way, each current source comes to be "ON" state in turn according to input code.

Two voltage levels VA and VB cross when input binary code changes from 0111 to 1000. Even in this case, change in the connection of current sources occurs only at one point.

Therefore, glitch generation is
Fig. 2 High speed segment decoder

Fig. 3 Relation of input binary code vs. voltage of each node
minimized.

4. DEVICE ACCURACY

In addition to the minimization of glitch energy, the advantage that accuracy requirement for each element is lessened arises.

The standard deviation $\sigma'$ of total 15 current sources becomes $\sqrt{15} \sigma$ when the standard deviation of one current source is $\sigma$.

This LSI is fabricated by our A-NSA bipolar IC process with polycrystalline silicon resistor on it. The accuracy of the ratio of this resistor value is less than 0.4% in a 3$\sigma$ standard deviation. And transistor's $\Delta V_{be}$ has a 3$\sigma$ standard deviation of 0.4mV making use of $12\mu m \times 12\mu m$ emitter size.

This leads to the result that 10 bits resolution is achieved without trimming of resistors.

5. ECL AND TTL COMPATIBLE INPUTS

One feature of the LSI is that this can handle both ECL and TTL level inputs only by connecting E/T terminal in Fig. 1 to either positive or negative rail.

Fig. 4 shows a circuit for ECL/TTL compatible input. Voltage of $V_B$ is 2.2V when point $\oplus$ is connected to GND line and point $\oplus$ to +5.0V line. And current value of current sources I1 and I2 are both 500$\mu$A. Resistors RL1 and RL2 are both 600 ohms.

When we use this DAC to correspond with ECL level inputs, we connect E/T terminal in Fig. 1 to point $\oplus$ in Fig. 4. And point $\ominus$ is connected to GND (0V) line and point $\oplus$ is connected to -5.2V line. Then switch (SW1) is "CLOSED" state and switch (SW2) is "OPEN" state. So transistors Q4 and Q5 operate as differential pair, but transistors Q6 and Q7 don't operate.

![Fig. 4 A circuit for ECL/TTL compatible input](image-url)
Voltage of VB is -2.8V. If Input voltage is higher than -1.3V, Q4 is "ON" state and Q5 "OFF" state, therefore, voltage of V4 is -300mV and that of V5 is 0V. When Input voltage becomes lower than -1.3V, Q4 turns "OFF" and Q5 turns "ON", then voltage of V4 becomes 0V and that of V5 becomes -300mV. Therefore input digital signal of ECL level is able to be transfered to internal circuits.

If we use this DAC to correspond with TTL level inputs, we connect E/T terminal to point B, and point A is connected to GND (0V) line and point A to +5.0V line. Then switch (SW1) is "OPEN" state and switch (SW2) is "CLOSED" state. So transistors Q6 and Q7 operate as differential pair, but transistors Q4 and Q5 don't operate.

Voltage of VB is 2.2V. If Input Voltage is lower than 1.5V, Q6 is "ON" state and Q7 is "OFF" state. When Input voltage becomes higher than 1.5V, Q6 turns "OFF" and Q7 turns "ON". Therefore input digital signal of TTL level can be transfered to internal circuits.

6. HIGH SPEED AMPLIFIER

Another feature of the LSI is that a high speed and wide-band amplifier is prepared on the same D/A converter chip as post D/A buffer as shown in Fig. 1. Fig. 5 shows a circuit of high speed amplifier. Q3, Q4, Q8 and Q10 are vertical PNP transistors. Maximum value of ft is 500MHz. So-called folded cascode circuit is used for an input stage to obtain wide gain band-width. Aperture correction is also avialble by using this amplifier.

This amplifier consumes only 17mW and has slew-rate of 50V/µS and band-width over 70MHz in unloaded condition.

![Fig. 5 High speed amplifier circuit](image-url)
7. PERFORMANCE OF THIS LSI

Fig. 6 and Fig. 7 show measurement examples of the differential gain and the differential phase sampled by 14.3 MHz clock. D.G. is 0.5\% and D.P. is 0.3\°.

The result of risetime measurement is shown in Fig. 8. In this case input binary code turns from 0000000000 to 1111111111. From Fig. 8 we calculated the settling time of this DAC to 1/2 LSB and that is about 10nS. Very high-speed D/A conversion has been realized.

Fig. 9 shows a glitch generation of input binary code from 0111111111 to 1000000000. Glitch energy is about 20 PVS. This value is much smaller than conventional DACs.
Fig. 10 Microphotograph of the DAC
8. CONCLUSION

A 10 bit 65 MSPS glitch-free video D/A converter LSI has been developed. The LSI can be widely used for High Definition TV and digital VTR application.

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10. REFERENCES


11. BIOGRAPHIES

Michinori Nakamura was born in Okayama, Japan, on May 22, 1955. He received the B.S. degree in electrical engineering from the University of Tokyo, Tokyo, Japan in 1978.

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