Abstract—This paper proposes a circuit to linearize the signal current and improve the distortion characteristics at the input of a current-mode circuit. Input voltage-to-current (V/I) conversion is carried out by a resistor that connects the signal source and the current input terminal of the current-mode circuit. The signal current flowing into the current-mode circuit through this resistor is distorted because of the signal-dependent voltage change at the current input terminal, and it is linearized by injecting a current that is proportional to the signal-dependent voltage change at the current input terminal, into the same current input terminal of the current-mode circuit. A current-mode sample-and-hold amplifier (SHA) that adopts the proposed scheme was fabricated and a 0.35-μm CMOS process was used to verify the effectiveness of the scheme. It operated from a 2-V supply voltage in the analog part and a 2.5-V digital part with a 100-MHz clock and realized a 77- and a 86-dB spurious-free dynamic range values for 0 and −40 dB of full-scale signal current level (±100 μA), respectively, of the 1-MHz signal input. More than a 13-bit equivalent SFDR for −14 to −4 dB of full-scale input was obtained, proving the effectiveness of the proposed scheme at realizing distortionless signal current processing.

Index Terms—CMOS, current-mode circuit, linearization, low power, low voltage, sample and hold.

I. INTRODUCTION

The breakdown voltage of transistors on an LSI chip becomes low as devices become small due to LSI process evolution. However, this means that analog circuits encounter the difficult requirement of achieving high precision due to rapid reduction of the signal dynamic range. It is estimated that in the future the allowable supply voltage for a precision analog circuit utilizing MOS transistors will be 1.8 V and eventually 1.5 V [1]. Therefore, it becomes necessary to develop analog circuits that are suitable for low-voltage operation and simultaneously possess high-precision, high-frequency and low-power characteristics.

The MOS current-mode circuit is one candidate because the maximum voltage swing which appears at gate terminals of current-mirror transistors is suppressed in a similar manner such that the signal current applied to an MOS transistor with its gate and drain terminals connected results in a small voltage change. Low-voltage and high-frequency operation are possible thanks to this small voltage swing [2]. However, it is difficult to realize high linearity due to the mismatch in current transfer ratio caused by the variation of device parameters in transistors, the node-voltage change depending on the signal, the finite output impedance of transistors, and the improper biasing to node voltages resulting in an imbalance of device terminal voltages.

The highest precision in current-mode circuits until now has been seen in SHAs and analog-to-digital converters (ADCs). A current-mode BiCMOS SHA [3] realized 57-MS/s and 60.4-dB SFDR for a 3-MHz input signal from a 3.3-V supply voltage. In [4], 30-MS/s and 48-dB SFDR for a 1-MHz input signal from a 1.5-V supply voltage was realized, while in [5], 35-MS/s and 55-dB SFDR for a 1.32-MHz input signal from a 1-V supply voltage was realized. Current-mode ADCs reported in [6] and [7] realized high-speed operation such as 50-MS/s and 135-MS/s for each channel; however, the resolution and therefore the distortion level remained 6-bit and 8-bit, respectively.

On the other hand, SHAs in [8]–[10] took the voltage-mode circuit approach and realized 40-MS/s and 50-dB SFDR for a 2-MHz input signal from a 1.2-V supply voltage, 50-MS/s and 58.2-dB SFDR for a 2.5-MHz input signal from a 1.5-V supply voltage, and 185-MS/s and 63-dB SFDR for a 45-MHz input signal from a 3.3-V supply voltage, respectively. The use of an improved source-follower buffer in a SHA is proposed to realize more than 70-dB SFDR with up to several tens of megahertz of the input signal in [11]; however, this effort still remains at the circuit simulation level. As a whole, the speed, SFDR and supply voltage realized in current-mode SHAs seem comparable to those in voltage-mode SHAs.

However, in the case of voltage-mode ADCs, a 10-bit resolution was realized in [12] with 60-MS/s and 65.8-dB SFDR from a 1.5-V supply voltage by adopting a Miller-capacitance based approach in a front-end SHA. Moreover, 14-bit resolution was realized in [13] with 20-MS/s and 82.3-dB SFDR from a 2.8-V supply voltage and in [14] with 12-MS/s and 103-dB SFDR from a 1.8-V supply voltage, both by utilizing calibration methods to cancel out offset and gain errors, that is, linearity errors. These calibration methods, however, cannot be applied to current-mode ADCs.

The above results show that current-mode ADCs need to gain improved accuracy and linearity without calibration to be claimed as candidates for future analog circuits. As the SHA is

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placed in front of the ADC and the conversion quality of the 
ADC largely depends on the SHA's performance, we have tried 
to improve the accuracy and linearity of a current-mode SHA 
with a linearized input V/I conversion scheme. The proposed 
scheme has been verified to have high accuracy through the 
evaluation of a fabricated SHA using 0.35-μm CMOS devices.

The rest of the paper is arranged as follows. In Section II, 
the base concept and its implementation by equivalent circuit 
models to realize highly linear V/I conversion is proposed. In 
Section III, assessment of performance parameters for the pro-
posed equivalent circuit models is described. Section IV shows 
the designed SHA circuit to which the proposed linearization 
scheme was adopted, and in Section V, some circuit simulation 
results including parameter variations are examined to deter-
mine the effectiveness of the scheme at the circuit simulation 
level. Section VI shows the results from the actually fabricated 
chip, and Section VII concludes this study.

II. METHOD TO REALIZE COMPLETE LINEAR V/I CONVERSION

A. Base Concept

From a system point of view, the use of LSIs that utilize 
current-mode processing throughout is rare, and a precision 
V/I conversion function is needed at the input. This function is 
commonly achieved with a resistor and an operational amplifier 
having a very high voltage gain. However, it is difficult to 
obtain a high voltage gain for an operational amplifier under 
low-supply-voltage and high-frequency conditions. Moreover, 
high voltage gain in an operational amplifier is always accom-
panied by stability problems.

The V/I conversion at the input of the current-mode SHA 
is achieved by using a negative feedback loop including a 
transconductance type op-amp as shown in Fig. 1(a) [5], [15]. 
However, an SfDR greater than 60 dB is still difficult to 
achieve. The major cause of this difficulty is the nonlinear 
V/I conversion occurring in the input circuit of the SHA.

Fig. 1(b) is an equivalent-circuit model for the input part of 
the SHA shown in Fig. 1(a). The nonzero and signal-dependent 
input impedance of the SHA is represented by the nonlinear 
impedance $Z_{IN}$ in the figure. The relationship between terminal 
currents and voltages in Fig. 1(b) is described as

$$\begin{align*}
i_1 &= G_{con}v_1 - G_{con}v_2 \\
i_2 &= G_{con}v_1 - G_{con}v_2
\end{align*}$$

where $G_{con} = 1/R_{con}$. We wish to make $i_2$ proportional only 
to $v_1$. We therefore add some value $G$ to the second term in 
the right-hand side of the second equation in order to obtain $i_2$ 
which is independent of $v_2$. The representation of such a modi-

$$\begin{align*}
i_1 &= G_{con}v_1 - G_{con}v_2 \\
i_2 &= G_{con}v_1 + (G - G_{con})v_2.
\end{align*}$$

Selecting a value $G$ equal to $G_{con}$, the $v_2$ element in the
second term of (2) becomes zero. This means that $i_2$ becomes 
completely independent of $v_2$; that is, precise V/I conversion 
of the input signal is achieved without being affected by any non-
linear $Z_{IN}$ at the node of the SHA by adopting a $G$ with a mod-
erate and achievable transconductance value. A circuit structure 
to realize (2) is shown in Fig. 2. As we need to add $Gv_2$ to the 
original $i_2$, a transconductance amplifier whose input is con-
nected to terminal 2 is introduced.

B. Implementation of the Concept in Equivalent-Circuit

Models

Fig. 2 is a conceptual figure; it should be implemented by an 
equivalent circuit such as that shown in Fig. 3. In Fig. 3, $G$ con-

selects a series connection of a low-pass filter with $R_{CL}$ and $C_{CL}$
and a transconductance $G_{0}$. The low-pass filter limits the 
frequency bandwidth of $G$. $R_{f}$ represents a combined resistor 
including the output resistances of the current source $J$ and the 
transistor $M_{1}$ with $R$ at its source in parallel, and $C_{in}$ is the par-
asitic capacitance at terminal ‘‘In’’ of Fig. 1(a). The operational 
transconductance amplifier “amp” appearing in Fig. 1(a) is re-
placed with a transconductance $G_{amp}$, an output resistor $R_{out}$
and a capacitor $C_{h}$. $C_{h}$ includes the sampling capacitor of the 
SHA. The $M_{1}$ with the degeneration resistor $R$ appearing in

When we calculate the impedance $Z_{\text{temp}}$, which is the negative feedback part of $Z_{\text{in}}$, the following relationship holds:

$$G_{\text{temp}} v_2 = \frac{v_a}{R_{\text{out}}} + j\omega C_h v_a$$

$$i_{\text{temp}} = G_{m1} v_a$$

(3)

where $v_a$ and $i_{\text{temp}}$ correspond to the voltage applied to the gate of $M_1$ and the current flowing into the drain terminal of $M_1$ in Fig. 1(a), respectively. From (3), we obtain

$$Z_{\text{temp}} = \frac{v_2}{i_{\text{temp}}} = \frac{1 + j\omega C_h R_{\text{out}}}{G_{m1} G_{\text{temp}}} R_{\text{out}}$$

$$= \frac{1}{G_{m1} A_0} \left(1 + j\frac{\omega}{\omega_0}\right) = R_{\text{eq}} + j\omega L_{\text{eq}}$$

(4)

where $A_0$ is the dc voltage gain of a transconductance amplifier, which equals $G_{\text{amp}} R_{\text{out}}$, and $\omega_0$ is $1/C_h R_{\text{out}}$. Equation (4) indicates that $Z_{\text{temp}}$ becomes a series connection of a resistor $R_{\text{eq}}$ and an inductor $L_{\text{eq}}$.

Therefore, the equivalent circuit in Fig. 3 is further modified to that shown in Fig. 4. By introducing a low-pass filter with $R_{xL}$ and $C_{xL}$, $G$ becomes band limited in frequency and it is written as

$$G = \frac{G_0}{1 + j\frac{\omega}{\omega_g}}$$

(5)

where $\omega_g = 1/C_{xL} R_{xL}$.

### III. PERFORMANCE ASSESSMENT

#### A. Stability

The addition of $G$, however, causes a positive feedback and hence requires care in order to maintain stability. It is seen in Fig. 4 that resistors $R_{\text{con}}$, the capacitor $C_{\text{in}}$ and the inductor $L_{\text{eq}}$ form an LCR parallel resonator, and that a transconductance amplifier $G$ in positive feedback configuration drives this resonator. Obviously, it has the configuration of a typical LC oscillator. $R_L$ and $R_{\text{con}}$ are omitted in this discussion. The condition required for the loop gain to maintain stability at resonant frequency becomes

$$|G| < G_{\text{con}}.$$  

(6)

In order to satisfy the condition in (6) even when values of $G$ and $G_{\text{con}}$ vary, $G$ is constructed as the series connection of a low-pass filter with $R_{xL}$ and $C_{xL}$ and a fixed transconductance $G_0$. The frequency characteristics are shown in (5). At low frequencies, the $|G|$ value becomes $G_0$; however, the $|G|$ value becomes smaller than $G_0$ at frequencies higher than $\omega_g$. Thus, $\omega_g$ is chosen several times below the resonant frequency of $L_{\text{eq}}$ and $C_{\text{in}}$ so that the magnitude $|G|$ becomes sufficiently small compared with $G_{\text{con}}$. Moreover, $G_0$ actually consists of a differential amplifier with a constant current source as its tail current. Thus, the $G_0$ value decreases due to clipping of the waveform after the transistor current becomes saturated when the input signal swing becomes large at high frequencies.

#### B. Frequency Characteristics

Below the resonant frequency of the parallel resonator in Fig. 4, the impedance is governed by the inductor part, and we use (4) as $Z_{\text{TN}}$. Then, $i_2$ becomes

$$i_2 = \frac{G_{\text{con}} v_1}{1 + Z_{\text{DS}} (G_{\text{con}} - G)} \approx \frac{G_{\text{con}} v_1}{1 + \frac{G_{\text{con}} - G}{G_{m1} A_0} + 1 + j\frac{G_{\text{con}} - G}{G_{m1} A_0} \frac{\omega}{\omega_0}}$$

(7)

$$G_{\text{con}} - G = G_{\text{con}} - G_0 \frac{1}{1 + j\frac{\omega}{\omega_g}}$$

(8)

We interpret the term $(G_{\text{con}} - G)$ as having the effect of reducing the $Z_{\text{TN}}$ value in (7). Equation (8) indicates that the effect of the $Z_{\text{TN}}$ value reduction will diminish as the signal frequency becomes higher than $\omega_g$. As a result, in the frequency range below $\omega_g$, the current error in $i_2$ decreases and the $-3$-dB frequency of $i_2$ increases compared with the conventional case without $G$.

#### C. Matching Issue Between $G$ and $G_{\text{con}}$

$G_{\text{con}}$ as well as $R_{xL}$ are polysilicon resistors in the actual IC circuit; therefore, their values change up to $\pm 20\%$. The low-pass filter in $G$ consists of a polysilicon resistor and a metal–metal capacitor. The change of the capacitor value is $\pm 10\%$, and the time constant $\omega_g$ of $G$ in (5) may change up to $\pm 30\%$ in total. As those two values $G_{\text{con}}$ and $R_{xL}$ change in correlation with each
other, $C_{\text{can}}$ decreases when $R_{\text{eqL}}$ increases. If $R_{\text{eqL}}$ increases by 20\%, the change in $\omega_g$ becomes $-30\% \sim -10\%$ depending on the $C_{\text{eqL}}$ change; if $R_{\text{eqL}}$ decreases by the same amount, it becomes $+10\% \sim +30\%$. $G_0$ in $G$ is realized by using a MOS differential circuit. The tail current for differential transistors does not change much because the bias current of this SHA is kept constant. This is because this SHA has been designed as a part of a pipelined current-mode ADC and it is necessary to keep the bias current constant in this ADC. We assume that the $G_0$ changes $\pm 10\%$ at maximum.

Unfortunately, we could not establish matching characteristics between $G$ and $G_{\text{can}}$ in this design. This implies that, in the extreme cases, $(G_{\text{can}} - G) = (G_{\text{can}} - (G_0/(1 + j(\omega/\omega_g))))$ in (8) becomes $(0.8G_{\text{can}} - (1.1G_0/(1 + j(\omega/0.9\omega_g))))$ and $(1.2G_{\text{can}} - (0.9G_0/(1 + j(\omega/1.1\omega_g))))$ due to changes of resistors, capacitors and the transconductance $G_0$. The coefficient of $\omega_g$ is selected so as to keep the difference between $G$ and $G_{\text{can}}$, as large as possible up to high frequencies in both cases. Improvement in realizing $G$ is necessary in the future such that $G_0$ and $G_{\text{can}}$ values change in correlation with each other.

D. Signal Dependent Parameter Changes

When the input signal current changes at the full-scale level, $G_{m1}$ changes because the current flowing in transistor $M_3$ and $R$ in Fig. 1(a) changes. Here, we assume that $G_0$ and $A_0$ do not change in the frequency range of interest because the voltage swing at terminal In is small. According to (4), $R_{\text{eq}}$ and $L_{\text{eq}}$ change in inverse relation to $G_{m1}$. The change of $L_{\text{eq}}$ causes a change in the resonant frequency at the SHA input stage, and hence care must be taken. However, the change of $G_{m1}$ has a definite range determined by the input signal range, that is, full-scale ac current swing. Moreover, the constant bias current $J$ is applied to $M_3$ and $R$ as seen in Fig. 1(a) and the change of $G_{m1}$ is small. Therefore, changes of $R_{\text{eq}}$ and $L_{\text{eq}}$, and of the error current and the frequency bandwidth in (7) are all small.

E. Noise

The addition of $G$ brings an additional noise to the SHA input stage. The input stage of the SHA becomes an LC resonator at high frequencies; however, our operating frequency is below the resonant frequency, which is necessary for the circuit to operate stably. Under this condition, the input stage becomes low impedance. The noise from $G_{\text{can}}$ is the current noise $i_G$, and its power-spectrum density per hertz is expressed as [16]

$$i_G^2 = 4kT \cdot F_G \cdot G_0$$

where $F_G$ is the “noise factor,” $k$ is Boltzmann’s constant and $T$ is the absolute temperature in Kelvin. The input resistor with its conductance $G_{\text{can}}$ and a resistor $R_{\text{eqL}}$ of a filter produce current noises and are injected to terminal 2 in Fig. 4 in parallel together with the noise current from $G_{\text{can}}$. Provided that the effect of the current noise from $R_{\text{eqL}}$ is included in $F_G$ and that $G_0$ is chosen to be the same value as $G_{\text{can}}$, the total noise power per hertz ($i_G^2$) becomes

$$i_G^2 = 4kT \cdot G_{\text{can}} (1 + F_G).$$

F. Nonlinearity of $G$

$G$ consists of a low-pass filter and a differential amplifier $G_0$, and it exhibits nonlinearity when the input voltage swing becomes large. However, when the input signal frequency is low, the voltage change at terminal 2 in Fig. 4 is less than several mVp-p. Even at high frequencies such as 10 and 30 MHz, the SPICE simulation indicates voltage changes of less than 30 and 80 mVp-p, respectively. The input voltage range of the differential amplifier is 150 mV in this design; therefore, the voltage change at terminal 2 is well within the input voltage range of a differential amplifier up to the Nyquist frequency. Moreover, the input signal for this differential amplifier begins to attenuate when the signal frequency exceeds $\omega_g$, which is 43 MHz in this design, due to the effect of the low-pass filter. Therefore, the influence of the nonlinearity of the differential circuit is small. However, improving the linearity of the differential amplifier by modifying the circuit such that it has two current sources that are connected to source terminals of differential transistors and a resistor between those source terminals seems to be effective especially at frequencies higher than 10 MHz. By this modification, the linear input voltage range of the differential amplifier increases. This type of the $G_0$ amplifier is also effective at improving the matching characteristics between $G_{\text{can}}$ and $G$ as discussed in Section III-C.

G. Example Calculation

In order to gain further insight, the resonant frequency, signal current errors at 1 and 10 MHz, and noise were calculated. In Fig. 3, we choose 5 kΩ for $R_{\text{eqL}}$, 0.74 pF for $C_{\text{eqL}}$, 15 kΩ for $R_{\text{out}}$, 0.5 pF for $C_1$, 2 mS for $C_{\text{amp}}$, and 0.5 pF for $C_{\text{in}}$. $G_{\text{can}}$ and $G_0$ were 0.5 and 0.55 mS, respectively, and the change in $G_{m1}$ was from 1 to 1.3 mS for the full-scale signal current change. We intentionally made the $G_{\text{can}}$ and $G_0$ values different. If $G_0$ is equal to $G_{\text{can}}$, the error term in (7) becomes zero in the frequency range of interest, and the effect of introducing the $G$ function can not be seen. Moreover, $G_0$ may not be the same value as $G_{\text{can}}$ in an actual circuit because we could not establish the matching capabilities between $G_{\text{can}}$ and $G_0$. Here, $G_0$ was set larger than $G_{\text{can}}$ to observe the more severe condition from the stability point of view.

Now, $R_{\text{eq}}$ and $L_{\text{eq}}$ in (4) become $33 \sim 26 \Omega$ and 0.25 $\sim 0.19 \mu \Omega$, respectively. This causes the resonant frequency of the SHA input stage to be 450 $\sim 516$ MHz. We assume that $C_{\text{in}}$, $C_1$, and $R_{\text{out}}$ do not change in this calculation. $G_{\text{amp}}$ is chosen as the worst case value. Then, $\omega_0$ and $\omega_g$ are $1.33 \times 10^8$ rad/s and $2.7 \times 10^7$ rad/s, respectively. When $f_{\text{in}}$ is 1 MHz, that is $\omega_{\text{in}} = 2\pi \times 10^6$ rad/s, substitution of $G_{m1} = 1$ mS and $A_0 = 30$ into $((1/G_{m1}A_0) \times (\omega_{\text{in}}/\omega_0))$ becomes 1.57. On the other hand, $\omega_{\text{in}}/\omega_g$ is 0.023 and $(G_{\text{can}} - (G_0/(1 + j(\omega_{\text{in}}/\omega_g))))$ becomes approximated to $G_{\text{can}} - G_0 = -0.05$ mS. The imaginary part in (7) becomes $7.85 \times 10^{-5}$, and this is 10 times smaller.
than that in the case without $G$. The current error in $\hat{i}_2$ is reduced by this ratio. Even when the input signal frequency is 10 MHz, $(1/G_{m1}A_0) \times (\omega_{in}/\omega_0)$ is 15.7 and $[(G_{con} - (G_0)/(1 + j(\omega_{in}/\omega_0)))$ becomes 0.12 mS. Still, the imaginary part and the error term in (7) becomes less than one-fourth compared with those in the case without $G$.

In the noise calculation, let us assume $F_G = 4$ though we do not know the exact value of $F_G$. Then, from (10) $\hat{i}_2$ becomes $4.14 \times 10^{-23}$ [A$^2$/Hz] at room temperature, or 300 degrees in Kelvin. When the bandwidth of the SHA is chosen to be 50 MHz, the noise current in total becomes $2.07 \times 10^{-15}$ [A$^2$]. The power of the full-scale signal current is $5 \times 10^{-9}$ [A$^2$] with a peak-to-peak current value of $\pm 100 \mu A$. The ratio between the input signal power and the noise power from the $G$ and $R_{con}$ is the signal-to-noise ratio (SNR), and it is calculated as 63.8 dB. If $F_G$ becomes larger than 4, the SNR deteriorates.

IV. CIRCUIT DESIGN OF SHA WITH THE INPUT CURRENT LINEARIZATION SCHEME

The designed circuit of the SHA is shown in Fig. 5. In [15], a similar concept and circuit were reported. As a result, a relatively good linearity was obtained, but, as the design was a preliminary one, the observed distortion level was only $-68$ dB for the 1.34-MHz input signal with $-5$ dB of full-scale current and the operating frequency was limited to 35 MS/s. It did not have a low-pass filter in $G$ and transistors as source degeneration resistors. The current difference between pseudodifferential channels was obtained by taking wired-or at the SHA output terminal.

On the other hand, the design in this paper used a differential-type clock driver with a resistor termination and optimized the size of sample switches and metal routing including supply lines in order to make the chip operate at 100-MHz clock speed. It introduced a low-pass filter in the $G$ function to stabilize the input part, source degeneration resistors and pMOS current mirrors for the output current composition. As a result, the real ability for linearization of this scheme and circuit has finally emerged.

For highly accurate and linear operation, it is necessary to eliminate error sources due to several nonideal effects. Signal-dependent current-transfer-ratio errors are caused by nonlinear $Vds$ changes for transistors in a current-mirror circuit due to the transistor’s finite output resistance. That kind of error is reduced by fixing node voltages in current-mirror circuits. In Fig. 5, transconductance amplifiers A11, A12 and an op-amp A1 are used to fix terminal voltages at terminals In1, A and Out1 in channel 1, respectively. The same kind of configuration is adopted in channel 2. A11 and A12 in channel 1 are simply differential transconductance amplifiers with nMOS differential transistors and a pMOS current-mirror to obtain a large phase margin. However, the power consumption is different because A11 needs to have high voltage gain, due to the fact that the load of M11 is a 2 k$\Omega$ resistor $R_{con1}$. A11 (or A21) consumes 1.2 mW, and A12 (or A22) consumes 0.4 mW of power. A1 and A2 in Fig. 5 are external to the SHA.

The threshold voltage ($V_T$) variation of a transistor is random in nature. However, the current-transfer-ratio error due to $V_T$ variation in a current-mirror circuit becomes small if the transconductance parameters of the transistors are small. This is the reason why source degeneration has been adopted throughout the circuit [5]. The W/L ratios of M11 and M12 in this design are $22 \mu m/0.8 \mu m$, and those of Mr11 and Mr12 are $10 \mu m/0.8 \mu m$. The Monte Carlo simulation result by SPICE indicates that the standard deviation $\sigma$ of the 250 $\mu A$ current in

Fig. 5. Designed SHA circuit with the input current linearization scheme.
a current-mirror circuit was 0.38% when 5 mV of $V_T$ variation occurred. The conventional way is to use transistors with long gate lengths. When the W/L ratio of $22 \mu m/2,1 \mu m$ is used for transistors in a current-mirror circuit, the transconductance of mirror transistors becomes comparable to that of this design. The standard deviation for 5 mV of $V_T$ variation became 0.42%. Note that the total gate area in this design is smaller than that of conventional approach, even though a similar standard deviation is expected. This is a feature of a current-mirror circuit with a source degeneration resistor. In addition to this, the pseudodifferential configuration is chosen in order to eliminate the influence of clock feed-through and channel charge redistribution from sample-and-hold (S/H) switches.

The linearization circuit that realizes conductance $G$ is shown in Fig. 5. The differential transconductance amplifier $G$ consists of transistors MC11 and MC21, two low-pass filters of $R_{PL}$ plus $C_{PL}$ and $R_{NL}$ plus $C_{NL}$, two constant current sources $I_0$, and one constant current source $2I_0$. $I_0$ is chosen to be 25 $\mu A$, and the transistor current becomes saturated if the input voltage difference is large. The voltage changes at terminals In1 and In2, however, are several mV at maximum, even for full-scale input signals at low frequencies. If offset voltages of A11 in channel 1 and corresponding A21 in channel 2 in Fig. 5 are in the range of several mV as well, those offset voltages do not affect the $G$ value, that is $G_0$ value in Fig. 4. $G_0$ stays nearly constant and the quiescent value of $G_0$ is set to be 0.5 mS.

The error-current correction at the input of the second stage (terminal A in Fig. 5) does not need to be taken into account because terminal A is driven by M12 with a degeneration resistor Mr12. M12 and Mr12 have a high output impedance, and the signal current flowing into terminal A has little error because the input impedance at A is small. A feedback loop with the operational amplifier A12 is used to lower the impedance at terminal A. The full-scale signal current level of this SHA (0 dBFS) is defined as $\pm 100 \mu A$, which flows into and out of terminals In1 and In2 in Fig. 5. In order to ensure that the change of transconductance in M11 and Mr11 depending on the input signal change is acceptable, the current source value J is chosen to be 250 $\mu A$.

V. CIRCUIT SIMULATION RESULTS

The designed circuit shown in Fig. 5 was SPICE-simulated using 0.35-$\mu m$ CMOS device parameters. The frequency characteristic of the absolute current value in M11 and Mr11 is the one to be simulated as shown in Fig. 6. Three different curves for circuits without $G$, with $G_0$ but without LPFs in $G$ (we refer to this as “$G_0$ only”), and with $G_0$ and LPFs in $G$ are shown in the figure. $G_0$ is chosen to be 0.5 mS. At 100 KHz of input-signal frequency, the current error is $-1.59 \mu A$ in the case without $G$ while it is reduced to $-0.04 \mu A$ for both the circuits with $G_0$ only and with $G_0$ and LPFs. When we assume $G_m$ and $A_0$ to be 1 mS and 30, respectively, as described in Section III-G, the signal currents that flow in M11 and Mr11 or in M21 and Mr21 in Fig. 5 are calculated as 98.36 $\mu A$ for the circuit without $G$. The simulated value coincides well with the calculated value. Moreover, simulation results show the linearizing effect to reduce the current error at frequencies below 10 MHz. The problem, however, is the gain peak for circuits with $G_0$ only and with $G_0$ and LPFs due to the existence of positive feedback as discussed in Section III-A. The peak might cause oscillation; therefore, it should be suppressed. A low-pass filter which consists of a resistor $R_{PL}$ and a capacitor $C_{PL}$, and another low-pass filter which consists of a resistor $R_{NL}$ and a capacitor $C_{NL}$, each of which has a time constant of 37 ns, have been introduced at inputs of MC11 and MC21 in $G$, respectively, as shown in Fig. 5. This means that $G$ becomes ineffective at frequencies above 43 MHz. The gain peak is greatly lessened and stable operation is guaranteed at the same time.

The linearity improvement including variation of $G$, $G_{0\text{en}}$ and the time constant of LPF was further verified by transient analysis followed by Fast Fourier Transform for checking harmonics when a full-scale differential signal at 1 MHz was applied to inputs of the SHA. The input signal current value is $\pm 100 \mu A$. The difference between the current that flows from Out1 terminal in channel 1 and the other current that flows from Out2 in channel 2 was analyzed and is shown in Fig. 7. The reason why the difference current was taken is that the circuit is configured as a pseudodifferential circuit. The third harmonic at
3 MHz is dominant; however, it changes depending on the variation of $G_0$, $G_{\text{con}}$, and the time constant of LPF. As discussed in Section III-C, there is a possibility for $(G_{\text{con}} - (G_0/(1 + j(\omega_1/\omega_2))))$ to become $(0.6G_{\text{con}} - (1.1G_0/(1 + j(\omega_1/0.9\omega_2))))$ (we refer to this as “$G_{\text{con}}$ Low”) and $(1.2G_{\text{con}} - (0.9G_0/(1 + j(\omega_1/1.0\omega_2))))$ (we refer to this as “$G_{\text{con}}$ High”) in the extreme cases. In Fig. 6, five results of simulations are plotted in overlapping format, and the third harmonic part is expanded to become the subfigure. When the designed circuit (1.0$G_0$ & 1.0$G_{\text{con}}$) is simulated, $-88.8$ dB of the third harmonic distortion level was obtained, which achieved 11.3-dB improvement compared with the case of “Without $G_{\text{con}}$”. When the designed circuit is modified such that $G_0$ becomes 1.1$G_0$, $\omega_1$ becomes 0.9$\omega_1$, and $G_{\text{con}}$ becomes 0.8$G_{\text{con}}$, the third harmonic distortion level is decreased to $-92$ dB. By the modification of $G_0$ to 0.9$G_0$, $\omega_1$ to 1.0$\omega_1$, and $G_{\text{con}}$ to 1.2$G_{\text{con}}$, the third harmonic distortion level deteriorates to $-80.7$ dB. However, this should be compared with the one labeled with “Without $G_{\text{con}}$ 1.2$G_{\text{con}}$” in $-72.5$ dB of distortion level in Fig. 7. Sufficient improvement can still be observed. As a whole, distortion tends to deteriorate when the $G_{\text{con}}$ value increases; that is, $R_{\text{con}}$ decreases. We might need to obtain matching between $G$ and $G_{\text{con}}$. This is a point for further study in our circuit design. However, these simulations indicate that introducing $G$ is effective at reducing the distortion.

VI. EXPERIMENTAL RESULTS

The SHA circuit in Fig. 5 was fabricated using a 0.35-μm CMOS process to demonstrate the effectiveness of introducing the linearization circuit, and to check what wide dynamic range is obtained for a current-mode circuit under a relatively low-supply-voltage condition. The chip microphotograph is shown in Fig. 13. The SHA forms a part of a larger chip. The supply voltage for the analog part is 2 V while that for the logic part, which supplies higher voltage to the gate of the sampling switches, is 2.5 V, and the power dissipation becomes 6 mW for the SHA in total. When $V_{\text{bias}}$ with a value of 1.206 V is applied as shown in Fig. 5, the dc input terminal voltages become 1.241 V and 1.244 V at the In1 and In2 terminals, respectively. This verifies that the offset has no influence on the $G$ value. As far as the chip operation is concerned, the tail current in $G_0$ is slightly increased because we needed to compensate for the poor current-sinking capability of current sources in operational amplifiers A11 (or A21) and A12 (or A22) in Fig. 5 caused by the incomplete design. Although we can not measure the $G_0$ value directly, it is estimated to be 0.55 mS by the circuit simulation. $R_{\text{con}}$ is decidable by the voltage gain measurement of SHA in sample mode and was 2.38 kΩ; therefore, $G_{\text{con}}$ was 0.42 mS. This situation is close to the case of “$G_{\text{con}}$ Low” described in Section V.

A. Gain versus Frequency

Fig. 8 shows the frequency characteristics of the SHA when it is in a sample mode. The outputs from the SHA are currents; they are converted to voltages by using operational amplifiers A1 and A2 as shown in Fig. 5. The voltage peak appears at a frequency near 30 MHz, and is close to the predicted one as in the case with $G_0$ and LPFs in Fig. 6. However, the amount of the peak in Fig. 8 (approximately 2.5 dB) is larger than that in Fig. 6 (approximately 1 dB), and further investigation is necessary to properly set the frequency characteristics.

B. SNR

Fig. 9 shows the SNR performance for this SHA. SNR was measured for different clock rates. The SNR values have some dependency on the input signal frequency bandwidth, that is, the clock frequency. It is considered that noises at virtual ground terminals of external op-amps affected because two external op-amps and a combiner are used to obtain the difference voltage after converting the differential output currents of SHA into differential voltages. As seen in Fig. 9, the wider the input signal frequency bandwidth is, the smaller the SNR value is. With a clock frequency of 20 MHz and full-scale input signal current to the SHA, the SNR exceeds 63 dB up to 9 MHz. This value is coincident with the estimated and calculated SNR value in Section II-E. With a clock frequency of 100 MHz and full-scale input signal current to the SHA, the SNR changes to values from 61 to 62 dB up to 25 MHz of the input signal. However, for a fixed clock frequency, SNR values do not change much from low frequency up to the Nyquist frequency.

**Fig. 8.** Input signal frequency versus SHA output signal voltage level (output voltage is converted from the SHA output current).

**Fig. 9.** SNRs in 20-MHz, 50-MHz, and 100-MHz clock signals.
C. Distortion

The proposed scheme should decrease the distortion of output currents to sufficiently low levels. We expect to have more than 80 dB of SFDR. It is predicted by the simulation in Fig. 7 that the third harmonic is a major distortion component when the input signal frequency is 1 MHz. In this SHA, the gate voltage boosting technique was not used to drive sampling switches. The supply voltage for the logic part is chosen to be 2.5 V so that the on-resistance of switches becomes low. However, we do not know to what extent the gate voltage of sampling switches should be elevated. Several curves in Fig. 10 are the measurement results of the SFDRs with different switch control voltages. The input signal level to this SHA becomes variable by preparing a signal with +5 dB of the full-scale level and 10-dB and 1-dB attenuators. A 1-MHz bandpass filter is placed at the output of the 1-MHz signal generator to reduce harmonics. The signal generator is the 14-bit DAC in actual. The differential signal at the SHA inputs is produced using a balun and has an SFDR of approximately 90 dB and more. This is shown by the curve labeled with “source” in Fig. 10. More than 80 dB of SFDR, that is, distortion characteristics, were obtained for the input signal level from −14 dB to −4 dB of the SHA full-scale level with a 100-MHz clock. Moreover, when the gate voltage of sample switches becomes less than 2.2 V, distortion deteriorates at higher levels of the input signal. This shows the necessity of using higher voltage or the voltage-boosting technique for the gate of sample switches.

D. Frequency Spectrum

In order to check that no other unwanted components exist throughout the frequency range up to the Nyquist frequency, the frequency spectrum of the output of the SHA was examined. The frequency spectrum of the SHA output when 1-MHz and 0 dB of full-scale input signal is applied to it is shown in Fig. 11. The frequency span from 0 to 50 MHz in a spectrum analyzer was observed. The clock frequency was 100 MHz. The largest unwanted component, the third harmonic, was −72.9 dB with respect to the fundamental as seen in Fig. 11. This is sufficiently small.

E. Full-Scale Level Transition

Fig. 12 shows the output waveform of the SHA with a 4.9-MHz full-scale wave at the input when the sampling clock is 10 MHz. This test is called the “envelope test.” The input signal is sampled approximately twice per one cycle and the full-scale level transition in sample mode can be observed at the peak amplitude part of the eye-like waveforms in 5 μS repetition as seen in the figure. The reason for choosing 10 MHz as a sampling clock was to see the transition clearly. When a higher frequency such as 49.9 MHz is used as an input with 100-MHz clock, the transition is filtered out, the observed waveforms become sinusoidal and the change can’t be recognized properly. Fig. 12 indicates that the envelope has no defect and the response is good. However, an overshoot was observed when SHA changed its state from the hold-mode to
the sample-mode. The peaking in the frequency characteristics appearing in Fig. 8 may influence this phenomenon.

F. Performance Comparison

The overall chip performances of the current-mode SHA in this paper and two other CMOS voltage-mode SHAs are compared in Table I. The SHA in reference 10 realized its performance in sacrifice with high power consumption and with the use of high supply voltage. Ours is superior to [9] in SNR, THD and the small full-scale input and to [10] in supply voltage, power, the small full-scale input and probably the distortion. The figure of merit is patterned after the formula (6) in [9], that is,

\[ FOM = \frac{P}{2\text{ENOB} \times f_s} \]  

(11)

where ENOB is the effective number of bits, \( f_s \) is the sampling rate, and \( P \) is the power consumption. The FOM of this work is the best.

VII. CONCLUSION

An effective linearization technique for input current using a resistor and a positive feedback is presented. The experimental results from the 0.35-μm CMOS chip show that this SHA achieved more than a 13-bit equivalent dynamic range. The result indicates that the linearization technique presented in this paper is effective for a current-based SHA under the constraint of low supply voltage and low power consumption. However, applying positive feedback causes a gain peak in frequency characteristics; therefore, a low-pass filter is inserted to reduce the amount of positive feedback at high frequencies. As a result, the effect of frequency bandwidth expansion becomes limited. As matching between \( C_{\text{on}} \) and \( C_F \) could not be established in this design, the effect of this linearization technique is also limited. Another problem is that the measured distortion differed from the value of the simulation. Further study to address these points is necessary.

REFERENCES


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